Abstract—We present an adaptable and reconfigurable software-defined payload (SDP) architecture that quickly enables multi-intelligence payload development of communications, radar and other missions. At the heart of Harris’ current SDP is an FPGA and interconnect fabric architecture that provides for a modular, flexible, scalable core capable of supporting a broad spectrum of missions with capabilities that can be customized for size, weight and power (SWaP) challenged platforms. The core fabric of the architecture provides the capability for rapid (~seconds) in-situ reconfiguration of the payload operational characteristics to support both communication and remote sensing collections in an operationally responsive manner. Illustrating the spectrum of capabilities evolving from this work, we present several selected mission areas. Specifically we discuss three SDPs, 1) a 100 Mbps-capable NASA CoNNeCT Ka-band software defined radio (SDR), 2) a SAR/ISAR X-band RADAR based on the NASA CoNNeCT SDR core, and 3) a tactical electronic warfare (EW) SDP providing signal characterization and location functions. Each payload concept relies heavily on the same FPGA core to configure specialized computing resources to conduct the missions within typical SWaP constraints, as well as, hardening the payload against spaceborne radiation environments. However, for near-space applications, dramatically increased integration can be achieved without sacrificing performance due to lower radiation environments expected for near-space. The SDP supports new and changing mission objectives, additional waveforms, and signal processing algorithms, thereby extending mission life and increases value by reducing mission life-cycle cost.

1. INTRODUCTION

Software defined radios (SDRs) have gained popularity due to the rapid reconfigurability of devices enabling the radio system to dynamically adapt to varying operational scenarios during a deployment or mission. Modern adaptation techniques include autonomous [1, 2] or cognitive methods [3], while traditional methods require external intervention (e.g. user entry or network control). Regardless of the adaptation method, the clear benefit is a single hardware platform that provides robust services over varying channel conditions and network connectivity, for example via adaptive modulation and/or waveform selection [4]. A key to the versatility of the SDR is that it relies on programmable computational hardware resources (e.g. DSP processors, FPGAs) rather than the dedicated circuitry typical in limited function MODEMS. SDRs are now being fielded, for example JTRS radios [5], to improve the efficiency of fighting forces. From a logistical standpoint a single multifunction unit reduces the costs associated with procuring, deploying and maintaining various field units and replacements while providing operational flexibility. The benefits of SDR technology are undisputed. These very same benefits afforded communication missions are now available to entire payload systems. However, the application of software-based dynamically reconfigurable DSP technology in the satellite domain has been limited. This is due to a number of interrelated factors such as:

- space environment survivability
- limited SWaP envelope
- reconfiguration requirements
- software deployment/management complexity

However, as discussed here, it is possible to overcome these barriers and provide a highly flexible capability using an in-situ dynamically programmable hardware core (figure 1-1) we term the software-defined payload (SDP) concept which is a more general view than an SDR.

An SDR is a specialized case of adapting just one sub-system of a typical multifunction payload. The SDP on the other hand, is a concept where the “personality” and capabilities of a payload are quickly (~ seconds), and possibly autonomously, reconfigured on-orbit (figure 1-2) to meet prevailing operational needs of the warfighters and INTEL community which would be the ultimate solution for operationally responsive space.

Figure 1-1 – Software Defined Payload Block Diagram

Figure 1-2: Notional example of dynamic reprogram of payload
This paper presents current work on a space qualified multi-mission payload system based on a hardware architecture that supports complete or partial reconfiguration of the processing elements. The computational elements we report on are primarily FPGA-based (figure 1-3), as FPGAs offer a balance in the cost/power/performance trade-space between ASICs and fully programmable processors. The approach utilizes recent advances in radio management software, signal processing hardware, and adaptable systems to meet not only radio systems needs, but those of other missions as well such as tactical EW, communication, IMINT (i.e. SAR/ISAR) and could be extended to other missions such as MOVINT (e.g. GMTI). The paper will also present the capability of the hardware elements operating in various sensor and communication instantiations to provide some performance benchmarks.

Figure 1-3 – Software Defined Payload Modularity

2. FPGA-BASED SOFTWARE DEFINED PAYLOAD

2.1 SDP Concept

Harris has been delivering multi-processor based Software Defined Payloads (SDP) since 1998 resulting in a development path from general purpose RISC processor-based architectures to today’s modern SDP architectures based on Xilinx Virtex FPGAs. In the mid-1990s, Harris began building and flying flexible processing elements for the space environment through the use of Reduced Instruction Set Computing (RISC) processors. With the advent of high performance FPGA processors, and techniques [6] which allow them to operate in space environments, the performance and reconfigurability necessary to tackle more complex processing scenarios has become increasingly viable.

The high-level block architecture of a generic SDP is illustrated in Figure 1-3. The basic elements of the system are the General Purpose Processing (GPP) Subsystem, the Signal Processing Subsystem, and the RF Front End Electronics Subsystem [6]. The GPP controls the payload operations and includes functions to load waveforms or configuration data. The GPP includes a common set of software infrastructure components that provide essential system management functions regardless of payload function through a consistent set of interfaces to configure, manage, and control the system hardware resources. The digital I/O cards provide standard interfaces to the vehicle, and can be customized for unique needs of a particular point application. The RF electronics are generally a separate package from the digital subsystems so that the RF functionality may be placed close to the aperture which tends to benefit overall system performance. The signal processing subsystem is a prime focus of this paper. The configuration of the signal processing subsystem dictates the function of the payload.

A fundamental tenet of the Harris approach has been the incorporation of standards and leveraging commercial off-the-shelf (COTS) hardware and software (figure 1-3). A commercially available real-time operating system (RTOS) provides the key interface between the hardware and operating environment (OE). The OE is based on the NASA Space Telecommunications Radio System (STRS) infrastructure. The system backplane uses the compact Peripheral Connect Interface (ePCI) standard. As a physical interface standard, Spacewire using the Remote Memory Addressing Protocol (RMAP) is employed to provide the intra- and intercomponent communications.

In prior work, limited to SDRs, it was found that requiring knowledge of the underlying physical architecture was a significant impediment to waveform porting and third party development in FPGA implementations [7]. Therefore, a key design objective in SDP is to enable third party development, while ensuring that the application will not harm the hardware or other payloads on the spacecraft. To achieve these opposing objectives, a set of Hardware Description Language (HDL) modules have been designed and implemented to abstract the hardware details of the SDR and provide a standard interface for payload developers and mission planners [7, 8]. Hardware abstraction is a key aspect of developing a software radio that promotes extensibility and new application development [8]. Additional work is needed to create abstractions of processing elements representing an entire spacecraft bus that uses a single or set of SDPs in order to promote the inclusion of third parties in evolving applications for reconfigurable spacecraft. We have taken some first steps in this direction with hardware abstractions of the SDR [8].

2.2 Harris’ V4 Space Processor

The V4 Space Processor (figure 2-1) is a core element of the SDP concept (figure 1-3) and provides a flexible compact Digital Signal Processor (DSP) module that delivers throughput rivaling dedicated ASIC-based solutions while providing an optimal balance in SWaP, cost and performance between dedicated function ASICs and fully programmable DSPs.
The V4 Space Processor is latest variant of a line of sustained R&D into radiation resistant reconfigurable computing elements suitable for space environments. It integrates high performance Virtex-4 FPGAs (256 GOPS), 1 GLOP general purpose DSP (SM320C6701), 256 MB RAM, flexible standard IO (IEEE 1149.1 JTAG, Dual Spacewire, four 1000 base CX 2.5 Gbaud serial ports, and SEU Circumvention logic along with demonstrated total dose hardness > 30 Krad, into a single conductively cooled 6U compact PCI (cPCI) form factor consuming ~ 30W. The SDRAM shown is used to hold the application data, and the SDRAM is portioned amongst several possible applications (e.g. typically 16) for a mission. However, the SDRAM can also be reprogrammed “at will” to provide updates during a mission are warranted. Harris used the V4 Space Processor as a core element in its space systems research and development programs such as the NASA CoNNeCT SDR (section 3), Imaging RADAR (section 4) and tactical EW (section 5).

Harris has also developed a small form factor module (2” x 2”, vol = 1 cu.in.) called a system-in-a-package (SiP) shown in figure 2-2. The SiP provides similar core functionality to that of a board-sized V4 space processor (figure 2-1), but has dramatically increased levels of integration. The Harris SiP represents a break-through in miniaturization technology and it has found use in miniature terrestrial software-defined radios [11], and is a step towards producing radios on a chip. While the SiP is not qualified for space operations, it could provide an enabling technology for the emerging class of high altitude surveillance platforms called near-space vehicles (NSV) [13]. In the near-term, NSVs are likely to share SWaP limitations similar to spacecraft. Further, given the anticipated CONOPs of NSVs a SWaP efficient multi-INT payload will likely be the preferred design option. Hence, with the low radiation environment for NSVs, a multi-INT/multi-mission payload design using the SiP or a fabric of SiPs as high performance computing elements is worthy of exploration.

At a top-level, the Harris SDR SiP is composed of 25 million programmable gates over 5 FGPAs, one DSP, two 125 Msps 14-bit ADCs, two 500 Msps DACs, 1 Gb RAM, 1 Gb Flash memory, USB 2.0, Ethernet, an Embedded Operating System (OS), and has equivalent processing capacity as a PC running at 160 GHz. The small size and short bus lengths allow lower drive current, exhibiting low power and negligible digital noise. The SDR SiP is currently at TRL 6, has completed LRIP, passed MIL-STD-883 for 500 temperature cycles (-40°C to 100°C), and 100 g shock and vibration. It provides high signal quality of -43 dB EVM for 64 QAM OFDM, demonstrated at over 200 Mbps.

Considering the resources on the SiP, high performance computing applications such as digital beamforming, MIMO, and STAP could be effectively hosted on a fabric of interconnected modules.

2.3 V4 Space Processor Radiation Hardness

For operation in a space environment the total ionizing dose (TID) and single event effects (SEE) require consideration. Additionally, the space environments are very different depending on the orbit (i.e. LEO, MEO, GEO, Molinya) and inclination. Shielding provides part of the solution, but shielding alone is often not practical. Hence, the V4 Space Processor is radiation hardened by design and part selection. The space processor, to meet the cost/performance objectives of the CoNNeCT program, is specified to sustain a minimum total dose of 30 Krad before performance degradation occurs. Impacting the total dose specification are tolerances required for variations in supply voltages, temperature, manufacturing tolerances and “end of life” issues for the circuitry.

Options exist for improving the total dose performance to 100 Krads. In particular, the current TID rating is primarily limited by the power converters which have failure modes above 30 krads. The SDRAMs are next most vulnerable part, rated to 50 krads. At doses > 50 krads the failures seen are mainly higher leakage currents, which require more frequent refresh operations. In both
cases, part selection can be altered to improve the total dose resistance of these functions. The rest of the parts are rated at > 100Krad which is feasible for most long duration LEO missions. However, for useful GEO mission life (e.g. 5 – 10 years), additional shielding is likely needed as part of the solution.

The primary space environment issues concerning this design are SEEs, which can be extremely problematic for programmable devices. SEEs are divided into three event classes

- Single Event Latchup (SEL)
- Single Event Upset (SEU)
- Single Event Transient (SET)

Our design philosophy has been to evaluate each part to ensure that they are immune from SEL (i.e. latch-up free), and to also characterize the SEU and SET events.

To mitigate the possible SEU and SET upset vulnerability the FPGAs V4 Space Processor uses two “on-board” methods:

- A “Watchdog ASIC” monitors each FPGA configuration memory during operation. The configuration is compared against the correct configuration (stored as a checksum in protected memory) and any detected errors are immediately corrected or “scrubbed”. The scrubber circuitry power consumption depends on the scrubbing rate. The user can set the rate for an environment to optimize power consumption.

- In addition, the logic within the FPGA is augmented by selected Triple-Modular Redundant (TMR) storage and logic. A special development tool is used to triplicate the appropriate logic in the application. Voters are used to isolate an error and "vote" it out of the result providing corrected data on the fly.

These two techniques together deliver very high (>99%) availability, verified by radiation testing conducted at the Berkeley and Texas A&M accelerator facilities while the V4 Space Processor performed as a high data rate MODEM.

The primary mechanisms have been employed to mitigate SEE in the SDRAM is Error Detection and Correction (EDAC) coding. EDAC is used to protect the memory contents and it can correct any error that exists in any single nibble of a 32-bit word. A dedicated scrubber, housed in the “watchdog ASIC”, reads every location in the SDRAM and validates the memory contents. The memory scrubbing rate is also programmable for possible power savings in various environments. Two spare SDRAM columns are provided in the memory array to allow the “watchdog ASIC” to “hotswap” these spare in for any other columns in the memory array as needed. We have used this memory architecture on several spacecraft.

Combined, these mechanisms reduce the cost of the system by using allowing the use of commercial parts that meet Class S reliability and this memory architecture has been validated on several spacecrafts [6]. Any additional components have been screened to ensure that they meet the requirements for outgassing, total dose, and latchup.

Of course, if the overall payload system required additional levels of fault tolerance the SDP concept is designed to support a sparing strategy such as “M-of-N” redundancy to improve system reliability. Typically, redundancy is implemented at backplane to “board level” module redundancy.

The following sections will present some selected applications of the V4 space processor.

### 3. V4 PROCESSOR IN A KA-BAND SDR

In support of the NASA Communications, Navigation, and Networking Re-configurable Testbed (CoNNeCT) program, Harris leveraged its existing software defined payload architecture to develop a high data rate Ka-band SDR. The CoNNeCT program is unique in that it will enable an SDR demonstration testbed on the International Space Station (ISS). Three different radios covering L-band, S-band, and Ka-band will be installed onboard the ISS and demonstrated as part of this program. The goal of this mission is to provide an operational testbed to demonstrate and exploit the features and benefits of SDRs on orbit. Many different datarates, waveforms, frequencies, and coding techniques will be demonstrated over the course of this mission.

![CoNNeCT Ka-band SDR Chassis](image)

The STRS compliant Ka-band radio delivered for this mission was based on the SDP architecture described above. Figure 3-1 shows the flight chassis designed around a 6U compact PCI open standard chassis which housed the majority of the payload elements. The Ka-band RF front end electronics is an external module to allow mounting at the antenna to optimize system performance. Figure 3-2 illustrates the overall payload architecture at the block level and figure 3-3 illustrates some of the actual hardware components. A main feature of the design is the
MODEM implemented with the Harris SDR based on the V4 processor.

The Harris SDR has the ability to transmit up to 100 Mbps of user data rate coded with ½ rate error correction coding on the return link to the NASA tracking and data relay satellite system (TDRSS), and receive up to 25 Mbps on the uplink from TDRSS at Ka-band. Sample BER curves from lab tests are shown in the figure (below) versus theory. The FPGAs of the V4 processor were used to provide as much of the radio’s functionality through the digital processor as possible. The radio digitally employed direct sampling of the intermediate frequency (IF) waveforms, a digital gain control algorithm, Doppler tracking filters, fine-tune frequency adjust, as well as the error coding, randomization, and other modem functions.

4. V4 PROCESSOR IN A RADAR PAYLOAD

4.1 PULSED CHIRP RADAR T/R

In order to demonstrate the multi-mission capability of the SDP architecture and build on the success of the CoNNeCT program, Harris embarked on a path to demonstrate an X-band radar capability in April 2010 [9]. Ten weeks later, as a result of significant reuse of key hardware and firmware building blocks, a stretch-mode X-band radar system was demonstrated as depicted in Figure 4-1. As shown in the figure the V4 Processor/MODEM is a key component in the payload architecture. Comparing figures 3-2, 3-3 and 4-1 shows that fundamentally the only hardware change from the CoNNeCT payload was the frequency translation into X-band, as opposed to Ka.

The CoNNeCT legacy FPGA firmware was modified to generate chirped linear frequency modulated (LFM) transmit radar waveforms. This was combined with a new external support RF X-band multiplier/frequency converter to provide a LFM waveform capability of up to 800 MHz of bandwidth. Various parameters such as pulse width, chirp rate, start frequency, stop frequency, pulse repetition rate (PRF), and number of pulses are easily modified given the software defined nature of the payload. Additionally, with alterations to the RF resources available, even entirely new waveforms could be dynamically configured into the FPGAs either from external sources or from the onboard memory. The ability to alter the RADAR payload so completely would provide a basis for spaceborne cognitive RADAR capabilities as well as supporting the dynamic mission needs for specific collection scenarios (e.g. resolution, EMI avoidance, spectral allocation, target/scene phenomenology).

The payload was designed for stretch mode processing in order to achieve a high downrange resolution without requiring commensurate wideband digitizers. The “dechirp on receive” compresses total RF bandwidth (e.g. 400 MHz) illuminating a range swath into a smaller instantaneous IF bandwidth (e.g. 100 MHz) which meets the sampling constraints of available space qualifiable high resolution ADCs. For this demonstration, a 12-bit ADC running at 300 MSPS was used to sample a 100 MHz IF bandwidth. RF bandwidths up to 800 MHz are supported...
which translates into a slant plane range resolution of approximately 0.25 m.

For the initial lab demonstrations, a transmit pulse was digitally generated, frequency converted and multiplied up to X-band, and then looped back into the X-band receiver, pulse compressed by a swept stretch mode LO and digitized. The range Impulse Response (IPR) and Multiplicative Noise Ratio (MNR) contribution were analyzed from the measured results [10]. Figure 4-2 below shows the IPR (blue) vs. the ideal MNR (red). Both the ideal and measured data used the Taylor weighted -35dB, nbar=5, per typical analysis methodology.

The raw uncalibrated measured data shows nearly ideal main lobe shaping and acceptably low non-ideal sidelobe artifacts. The only significant sidelobe energies of interest are the near-in lobes adjacent to the main lobe. These are due to deterministic phase errors caused by RF filter group delay changes near the edges of the passbands, and are easily removed through simple radar calibration techniques which on-board test could dynamically measure and remove. However, even with these effects unmitigated the raw data exhibited an -23 dB MNR which meets typical allocations for RF radar electronics hardware.

The ISAR test set-up provided for multiple polarizations (HH, VV, Diagonal/Diagonal). The target is complex consisting of multiple corner reflectors. The RADAR SDP parameters were varied during the measurements and the capability of providing 0.25m resolution was demonstrated. This is typically 3x better than commercial SAR systems on-orbit today.

The ISAR images of the P38 lightning scale model were varied in RF bandwidth and synthetic aperture length to show multiple ISAR pictures at varying resolutions (figure 4-4). For these measurements, the frequency chirp slope rate was set to 40 MHz/usec and the pulsewidth was changed from 5 to 20 usec. At the highest resolution of 0.25m, the proportionate details of the plane’s twin engines and fuselages, pilot cockpit, tail section, and wing-mounted fuel tanks were clearly recognizable. This is impressive since the scale model is similar in size to a small class UAV. As one can see in the ISAR images, this radar measured resolution performance could be used to identify UAV types through feature recognition.

4.2 Pulsed Chirp Radar (ISAR Results)

The NASA CoNNeCT hardware and firmware were leveraged again to create the core processing module of an ISAR RADAR payload. ISAR is inverse SAR where the target provides the rotation to obtain the cross range resolution, rather than the measurement platform. To again illustrate the multi-mission capability of the Harris SDP a simulated ISAR collect was performed on a ¼ scale model P-38 aircraft in an anechoic chamber (figure 4-3).

Figure 4-3: ¼- scale model of P-38 Lightening mounted in chamber for ISAR Tests

Figure 4-4: ISAR images from V4 based SDP payload at various resolutions (a) 1 m, (b) 0.5 m , (c) 0.25 m

5. V4 PROCESSOR IN A TACTICAL EW PAYLOAD

As part of the ongoing effort to evolve programmable payloads for spacecraft Harris undertook a study using the V4 Space Processor to host a variety of previously developed and at-speed tested tactical EW algorithms which measure parameters such as

- Power Level
- Frequency: Center, Bandwidth, Slopes
- Modulation on Pulse (MOP)
- Timing: ToA, Pulsewidth
- Geolocation: AoA

During the study, a wide-band digital receiver was
designed and optimized for maximum instantaneous bandwidth (IBW), detection sensitivity, and parametric performance. The two primary waveform targets of interest were wide-band pulse (pulse) and narrow band modulated contiguous waveform (CW).

Harris developed two primary algorithm instantiations, a 2-channel 300 MHz IBW (figure 5-1) supporting TDOA-based geolocation and 6-channel 100 MHz IBW (figure 5-2) supporting monopulse-based geolocation. Both versions are based on wide-band channelizers, matched resolution bandwidth (RBW) channels, and digital processing gain. The V4 processor was used as the computing elements for the architectures shown. The RF tuners and data acquisition sub-systems were “off board” in separate space qualifiable modules. Efforts are currently underway to port the 100 MHz version of the waveform to Harris multi-mission SDP hardware.

Regardless of IBW, the detection and characterization approach is broken into the two distinct functions of detection and set-on. Detection is defined as declaring the presence of a signal, where the set-on function is used for AoA determination and parametric characterization of the signals. Two different detection engines, pulsed and CW, were developed to optimize detection performance, under a stringent Probability of False Alarm (Pfa) constraint, for a given waveform type. The EW payload measurements and functional module executing the measurement are listed in table I below.

![Figure 5-1: 2-Channel 300 MHz V4 Processor EW system](image)

![Figure 5-2: 6-Channel 100 MHz V4 Processor EW system](image)

To provide a reference for the performance achieved, in pulsed signal mode a minimum detectable threshold (MDT) of 16 dB SNR coherent in 20 MHz reference BW with only 100 false alarms per second was achieved (figure 5-3). While for CW mode, an MDT of 1.5 dB SNR coherent in 10 MHz reference BW with 100 false alarms per second was achieved. In each case we can lower the SNR in the reference BW, by matching to the signal BW. This operation has been achieved using a layered approach of successively narrower filter banks to sub-divide channels.

The AoA in each configuration is determined in the set-on engine and is based on variants of Harris’ Blind Signal Sorting (BSS) algorithms. The approach relies on an eigensolver technique to produce weights that, when post-processed with a calibration grid, yield the individual emitters angle-of-arrival. The methods used in the estimation of the steering vector can also be applied in a mono-pulse based receiver.

![Figure 5-3: Example of detection performance (100 ns PW) versus SNR for FAR of 100 false alarms/sec versus polarization](image)

Overall, the detection and set-on functions were designed into a modular frame-work, where different sub engines could be integrated to provide a different mission utility. In a similar fashion new detection engines could be developed for processing of a different class of waveforms.

### 6. CONCLUSIONS

The adaptability and configurability of this space-qualified SDP architecture quickly enables the payload development of communications, radar and other missions.

An example of this is shown in the multi-mission hardware configurations (figure 6-1). These three functions have been described in this paper, and if desired with small expansion of on-board payload allocation all the RF support to enable the entire mission within a single payload can be accommodated.

Analysis has shown that the V4 processor can be completely reprogrammed through industry standard interfaces and begin operating the new configuration in less than 15 seconds. This level of adaptability yields unprecedented dynamic mission flexibility for an operationally responsive payload. It also opens the possibility to consider on-board autonomous controllers to
manage the sensor time lines to address prioritized mission elements from analysts.

In addition, the power of this software defined aspect of this payload platform supports new and changing mission objectives, additional waveforms, data protocols, and signal processing algorithms, thereby extending mission life and increasing value by reducing the overall life-cycle cost.

This software defined payload architecture has been used to quickly and cost-efficiently develop communications and radar systems.

Leveraging software defined payload/radio technology to meet a variety of space mission needs is now within reach and has been demonstrated. By using Harris’ high-TRL software defined payload architecture and software environment, the cost, risk, and schedule of implementing new payload mission needs has been greatly reduced.

Figure 6-1: A Family of common processor core payloads

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8. REFERENCES


